



Product Specification

M240UP01 V0 open cell

AU OPTRONICS CORPORATION

(V) Preliminary Specification

() Final Specification

Module	24" WUXGA Color TFT-LCD
Model Name	M240UP01 V0 Open Cell

Customer	Date
_____	_____
Approved by	
_____	_____
Note: This Specification is subject to change without notice.	

Checked & Approved by	Date
Prepared by	
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Desktop Display Business Unit / AU Optronics corporation	

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Record of Revision

Version & Date	Page	Old Description	New Description	Remark

1. Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not press the or pat the panel surface by fingers, hand or tooling.
- 8) Please handle TFT cell with care. The FPCs can only sustain for quite limited stress.
- 9) The cell package tray is packed in clean room. Please do pack & unpack it in clean room.
- 10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of TFT cell.

2. General Description

This specification applies to the 24 inch-wide Color TFT-LCD open cell M240UP01 v.0. The screen format is intended to support the WUXGA (1920(H) x 1200(V)) screen and 16.7M colors (RGB 6-bits + Hi-FRC data). The input signals are VESA standard analog RGB and DVI-D interface compatible.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 °C condition:

Items	Unit	Specifications
Active Area	[mm]	518.4(H) × 324(V)
Pixels H x V		1920 × 3(RGB) × 1200
Pixel Pitch	[mm]	0.270(per one triad) × 0.270
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		TN Mode, Normally White
Optical ResponseTime	[msec]	5 ms(Typ)
Nominal Input Voltage VCC	[Volt]	+5.0 (Typ)
Power Consumption (VCC line)	[Watt]	8(Typ)
Weight	[Grams]	804.7 (Typ)
Electrical Interface		VESA standard Analog RGB ; DVI-D (HDCP1.1)
Surface Treatment		Anti-glare type, Harness 3H
Support Color		16.7M colors (RGB 6-bits + HiFRC data)
Plug & Play		VESA DDC2B/2Bi/2B+/CI ²
Compability		PC/MAC
Max. Firmware Code Size	[byte]	64K+32K
Max. Pixel Clock	[MHz]	165 MHz
Auto Adjustment		Auto Color, Size & Phase ²
RoHS Compliance		RoHS Compliance

¹ With AUO standard firmware

² With AUO standard power module & firmware



2.2 Optical Characteristics

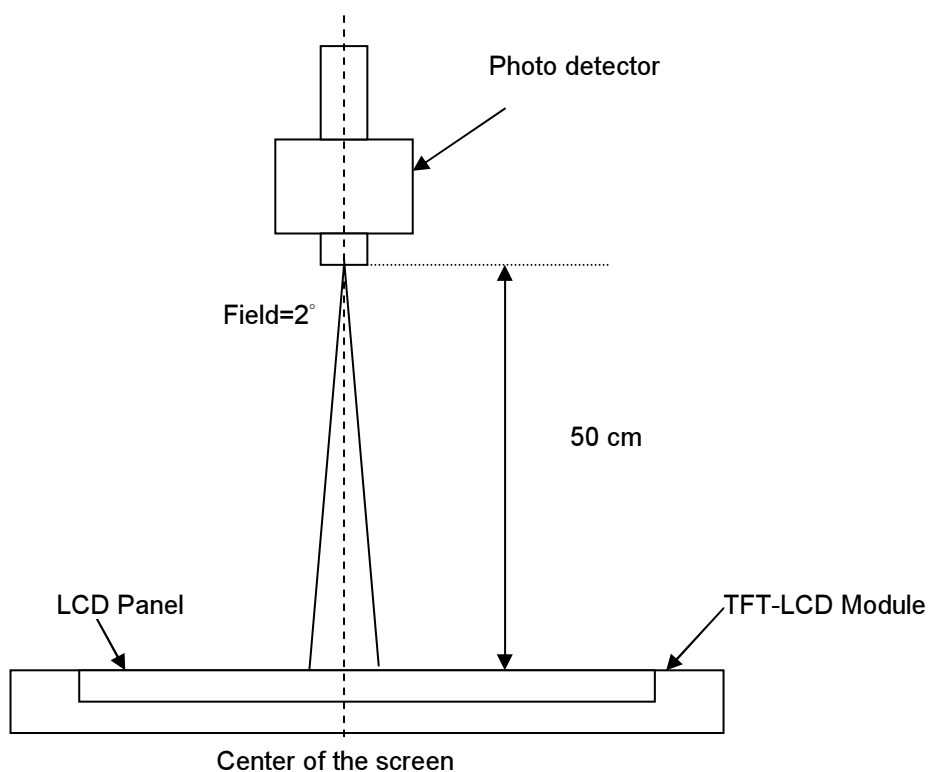
The optical characteristics are measured under stable conditions at 25°C (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
Optical Response Time	[msec]	Rising	-	3.8	6.1	1, 3
		Falling	-	1.2	1.9	
		Rising + Falling	-	5	8	
		Grey to Grey (avg.)	-	2	-	
Cross Talk (At 75Hz)	[%]		-	-	1.5	2
Flicker	[dB]		-	-	-20	4

Optical Equipment: BM-5A, BM-7, PR880, or equivalent

Note 1: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.



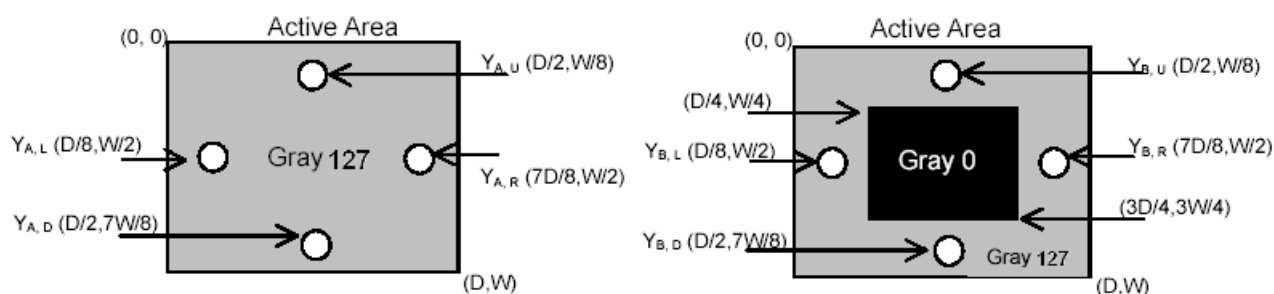
Note 2: Definition of Cross Talk (CT)

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where

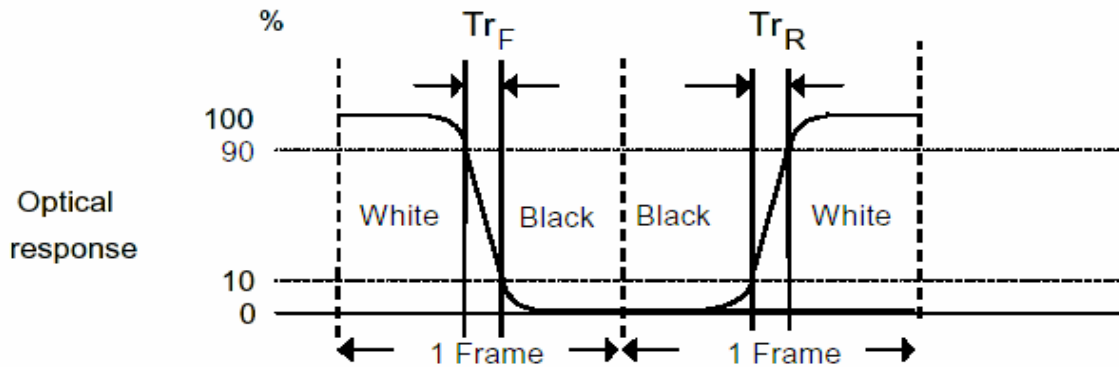
Y_A = Luminance of measured location without gray level 0 pattern (cd/m²)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m²)

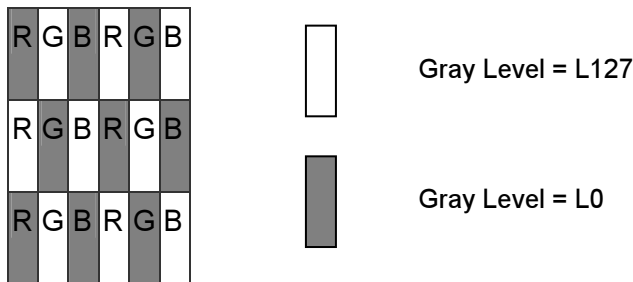


Note 3: Definition of response time:

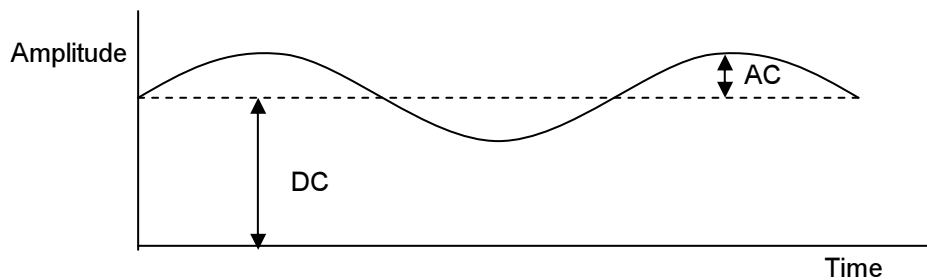
The output signals of photo detector are measured when the input signals are changed from “Full Black” to “Full White” (rising time), and from “Full White” to “Full Black ”(falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 4: Subchecker Pattern



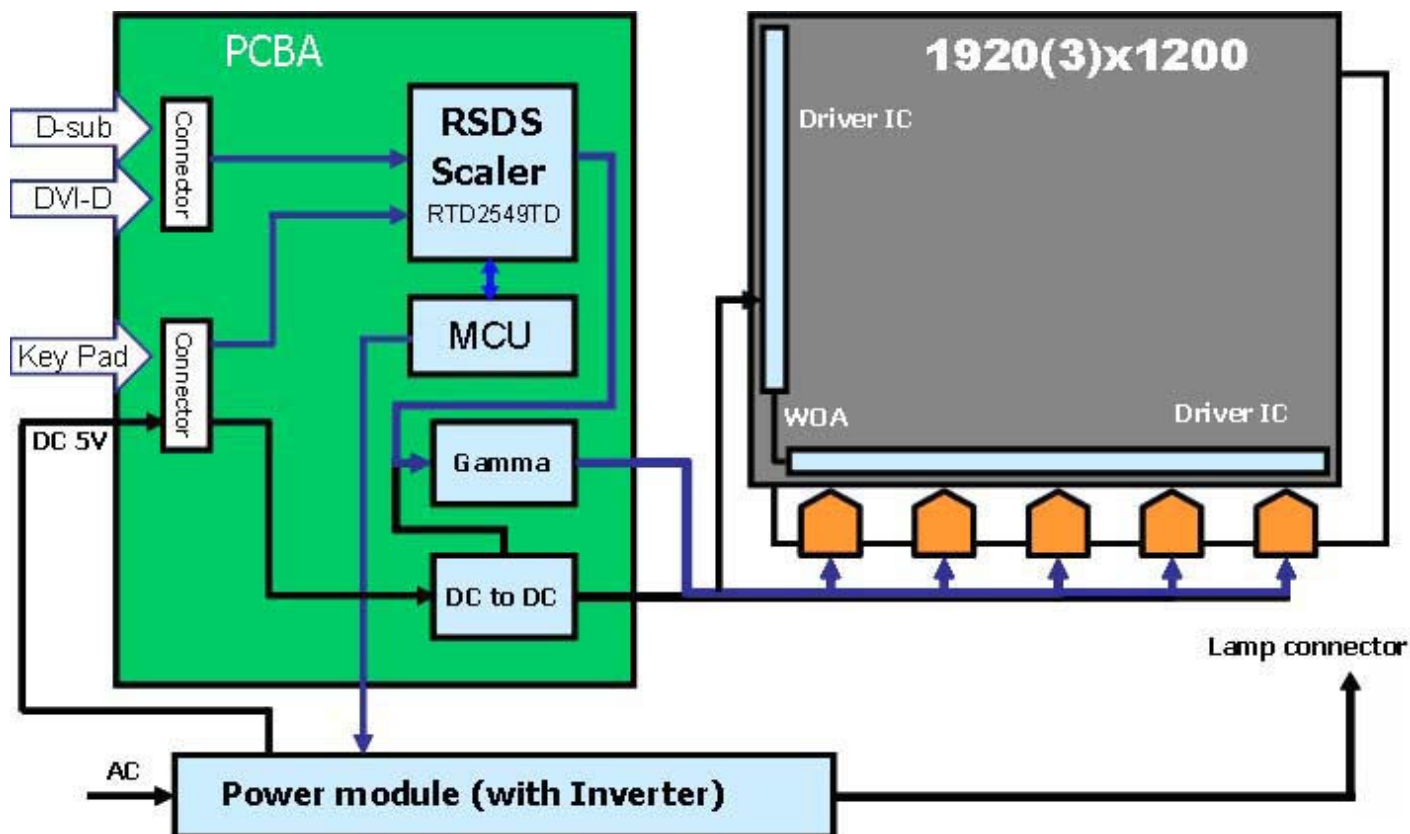
Method: Record dBV & DC value with (WESTAR)TRD-100



$$\text{Flicker (dB)} = 20 \log \frac{\text{AC Level(at 30 Hz)}}{\text{DC Level}}$$

3. Functional Block Diagram

The following diagram shows the functional block of the 24.0 inches wide Color TFT-LCD Module:



4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min.	Max.	Unit	Conditions
Logic/LCD Drive Voltage	VCC	-0.3	+5.25	[Volt]	Note 1, 2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min.	Max.	Unit	Conditions
CCFL Current	ICFL	0	8.0	[mA] rms	Note 1, 2

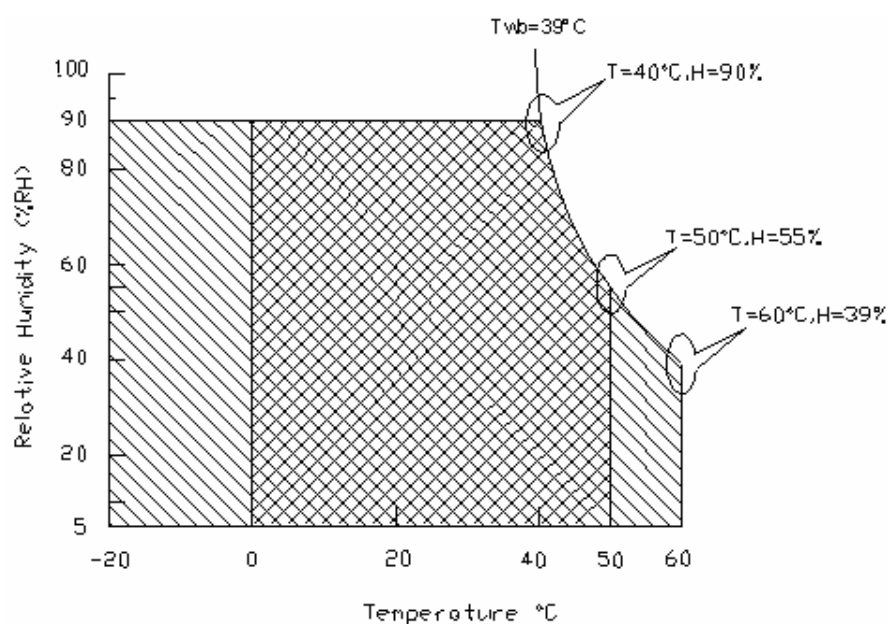
4.3 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	90	[%RH]	
Storage Temperature	TST	-20	+60	[°C]	
Storage Humidity	HST	5	90	[%RH]	

Note 1: With in Ta= 25°C

Note 2: Permanent damage to the device may occur if exceed maximum values

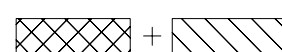
Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



Operating Range



Storage Range





5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows:

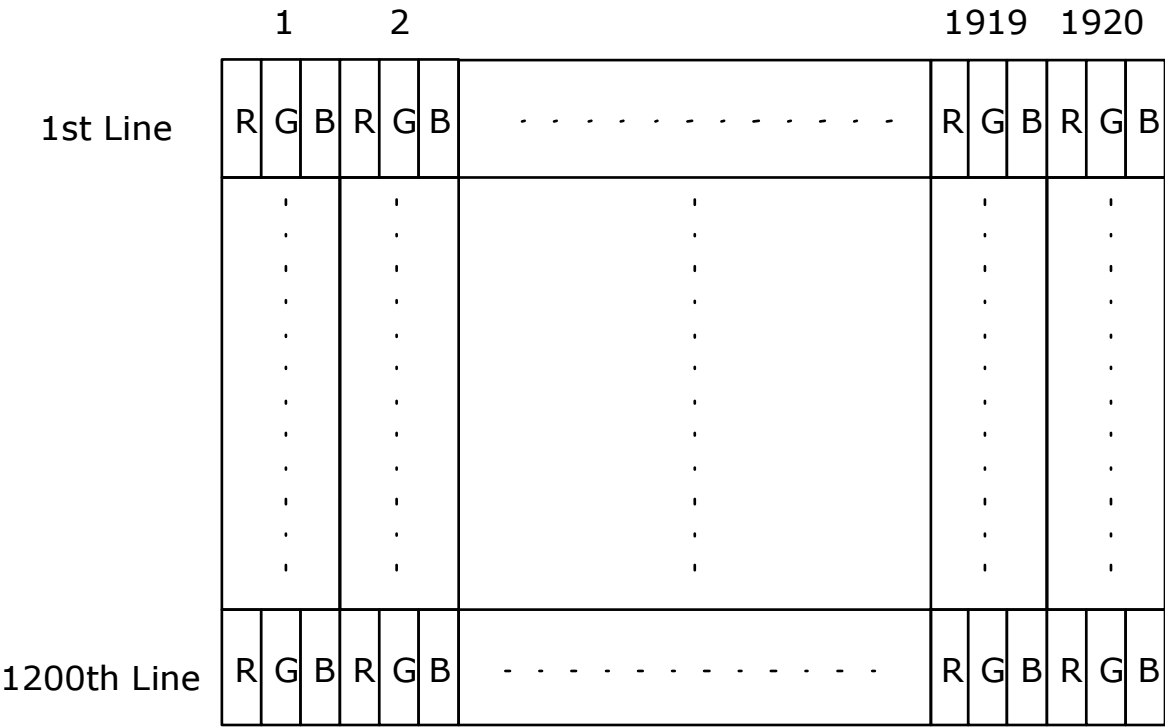
Symble	Parameter	Min.	Typ.	Max.	Unit	Condition
VCC	Logic/LCD Drive Voltage	4.75	5.0	5.25	[Volt]	Load Capacitance 20uF
ICC	Input Current	-	1.6	2.4	[A]	VCC= 5.0V, All Black Pattern
PCC	VCC Power	-	8.0	12	[Watt]	Note 1, VCC= 5.0V, All Black Pattern
VCCrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	[mV] p-p	
PS	Power Saving	-	0.3	0.5	[Watt]	VCC= 5.0V

Note 1: The variance of VCC power consumption is $\pm 10\%$.

6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



6.2 Signal Description

➤ Power / OSD Connector (J1)

PIN#	Signal Name	Description
1	VCC	DC 5V
2	BKLT_ADJ	Light adjust for the DC/AC inverter(PWM)
3	VCC	DC 5V
4	BKLT_EN	Enable for the DC/AC inverter
5	VCC	DC 5V
6	AUDIO_EN	Enable audio power control signal
7	VCC	DC 5V
8	MUTE	Mute audio
9	GND	Ground
10	VOLUME	Adjust audio volume (PWM)
11	GND	Ground
12	Key_Power	Power on/off function
13	GND	Ground
14	MENU	OSD menu on/off function
15	GND	Ground
16	PLUS	OSD plus selection function
17	S/PDIF	Audio control signal
18	MINUS	OSD minus selection function
19	I2CSDA	I2C SDA
20	DOWN	OSD down selection function
21	I2CSCL	I2C SCL
22	UP	OSD up selection function
23	SD0	Audio data
24	SELECT	OSD item select function
25	WS	Audio control signal
26	SOURCE	OSD item source function
27	SCK	Audio control signal
28	LED_A	LED Amber for the sleep mode
29	MCK	Audio control signal
30	LED_G	LED Green for the full mode

➤ DVI-D / D-sub Connector (J2)

PIN#	Signal Name	Description
1	DATA2/4 Shield	Shared shield for TMDS link #0 channel #2 and link #1 channel #1
2	GND	Ground
3	DATA2+	TMDS link #0 channel #2 differential pair
4	DVI_5V	+5V signal provided by the system to enable the monitor to provide EDID data when the monitor circuitry is not powered.
5	DATA2-	TMDS link #0 channel #2 differential pair
6	HPD	Host Plug Detect ; Signal is driven by monitor to enable the system to identify the presence of a monitor.
7	GND	Ground
8	GND	Ground
9	DATA1+	TMDS link #0 channel #1 differential pair
10	DDC Data	The clock line for the DDC interface
11	DATA1-	TMDS link #0 channel #1 differential pair
12	DDC Clock	The data line for the DDC interface
13	DATA1/3 Shield	Shared shield for TMDS link #0 channel #1 and link #1 channel #0
14	GND	Ground
15	DATA0+	TMDS link #0 channel #0 differential pair
16	VCC	DC 5V
17	DATA0-	TMDS link #0 channel #0 differential pair
18	HDMI_HDP	2D reserved I/O
19	DATA0/5 Shield	Shared shield for TMDS link #0 channel #0 and link #1 channel #2
20	2D_SW	2D reserved I/O
21	Clock+	TMDS clock differential pair
22	DVI_CONN	2D reserved I/O
23	Clock-	TMDS clock differential pair
24	GND	Ground
25	Clock Shield	Shield for TMDS clock differential pair
26	VSync	Vertical synchronization signal for the analog interface
27	B_GND	Ground for the analog blue signal
28	HSync	Horizontal synchronization signal for the analog interface
29	BIN	Analog Blue signal
30	GND	Ground
31	G_GND	Ground for the analog green signal
32	SDA	The data line for the DDC interface
33	GIN	Analog Green signal



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34	SCL	The clock line for the DDC interface
35	R_GND	Ground for the analog red signal
36	PC_5V	+5V signal provided by the system to enable the monitor to provide EDID
37	RIN	Analog Red signal
38	VGA_CON	Video cable connected detect signal (host connect this pin to ground)
39	GND	Ground
40	GND	Ground

Note 1: For DVI-D cable part:

- a. DVI differential pairs (DATA-/+) impedance 100+/-10 Ohm.
- b. DVI differential pairs (DATA-/+) should twist wire.

Note 2: For D-sub cable part:

- a. R/G/B impedance 75+/-10 Ohm

6.3 The input data format

The input data format is followed the VESA Vedio Signal Standard. In each RGB termination is described as following table.

	Values
Max Luminance Voltage Input Data = (FFh)	0.700 Volts +0.070 /-0.035 volts
Min Luminance voltage Input Data = (00h)	0.000 Volts
Video Channel Rise/Fall Time Max	25% of minimum pixel clock period
Maximum Settling Time after overshoot/undershoot	30% of minimum pixel clock period averaged over 100 waveforms to 5% final full-scale value.
Monotonic	Yes
Resolution	1 LSB
Integral Linearity Error	± 1 LSB
Differential Linearity Error	± 1 LSB
Video Channel to Video Channel Mismatch	6% of any video output voltage over the full voltage range
Video Noise injection ratio	± 2.5 % of Max Luminance Voltage
Video Channel to Video Channel Output Skew	50% of minimum pixel clock period
Overshoot/Undershoot	± 12 % of step function voltage level over the full voltage range



The Synchronization (Hsync and Vsync) Signal format is described as following table.

	Min.	Max.
Driver Logic Level "1"	2.4 Volts	5.5 Volts
Driver Logic Level "0"	0.0 Volts	0.5 Vots
Driver High Level Output Current	8mA	
Driver Low Level Output Current	8mA	
Receiver Logic Level "1"	2.0 Volts	
Receiver Logic Level "0"		0.8 Volts
Fall Time Max		80% of minimum pixel clock period
Rise Time Max		80% of minimum pixel clock period
Monotonic Rise/Fall Voltage range	0.5-2.4 Volts	
Overshoot/Undershoot		30% of high level signal voltage range No signal excursions allowed in the 0.5-2.4 volt voltage range
Jitter (Measured between Hsync pulses)		Over the frequency spectrum: One half of the difference between the maximum and minimum interval between Hsync pulses measured over 100,000 intervals shall be less than 15% of the pixel clock, 0Hz to max. horizontal refresh rate at all image formats, worst-case screen patterns.

- ✧ LSB: Least Significant Bit
- ✧ Monotonic
 1. The property of either never increasing or never decreasing in reference to the slope of a transient response.
 2. A constant slope value containing no inflection points.
- ✧ Sync: Synchronization Signals

For more details, please refer to VESA (**Video Electronics Standards Association**) Video Signal Standard.

6.4 Signal Electrical Characteristics

➤ Power / OSD interface (J1)

Pin#	Name	Type	Min.	Typ.	Max.	Unit	Remark
1	VCC		4.75	5.0	5.25	V	
2	BKLT_ADJ	High (Max.)		VCC		V	Internal serial 2.2K Ohm
		Low (Min.)		0.3		V	Internal serial 3.2K Ohm
3	VCC		4.75	5.0	5.25	V	
4	BKLT_EN	High (On)		VCC		V	
		Low (Off)		0.3		V	Internal serial 10K Ohm
5	VCC		4.75	5.0	5.25	V	
6	AUDIO_EN	High (On)	2.65		3.3	V	-4mA
		Low (Off)	GND		0.45	V	5mA
7	VCC		4.75	5.0	5.25	V	
8	MUTE	High (On)	2.65		3.3	V	-4mA
		Low (Off)	GND		0.45	V	5mA
9	GND						
10	VOLUME	High (Max.)	3.2			V	
		Low (Min.)			0.1	V	4mA
11	GND						
12	Key_Power	Active		0		V	
13	GND						
14	MENU	Active		0		V	
15	GND						
16	PLUS	Active		0		V	
17	S/PDIF						
18	MINUS	Active		0		V	
19	I2CSDA						
20	DOWN	Active		0		V	
21	I2CSCL						
22	UP	Active		0		V	
23	SD0						
24	SELECT	Active		0		V	
25	WS						
26	SOURCE	Active		0		V	
27	SCK						
28	LED_A	LED Amber for the sleep mode		3.1		V	Internal serial 68 Ohm
29	MCK						
30	LED_G	LED Green for the full mode		3.1		V	Internal serial 68 Ohm



➤ DVI-D / D-sub interface (J2)

Pin#	Name	Type	Min.	Typ.	Max.	Unit
1	DATA2/4 Shield					
2	GND					
3	DATA2+					
4	DVI_5V					
5	DATA2-					
6	HPD					
7	GND					
8	GND					
9	DATA1+					
10	DDC Data					
11	DATA1-					
12	DDC Clock					
13	DATA1/3 Shield					
14	GND					
15	DATA0+					
16	VCC					
17	DATA0-					
18	HDMI_HDP					
19	DATA0/5 Shield					
20	2D_SW					
21	Clock+					
22	DVI CONN					
23	Clock-					
24	GND					
25	Clock Shield					
26	VSync	High	2.0		5.0	V
		Low	GND		0.8	V
27	B_GND					
28	HSync	High	2.0		5.0	V
		Low	GND		0.8	V
29	BIN			700		mV
30	GND					
31	G_GND					
32	SDA	High	2.0		5.0	V
		Low	GND		0.8	V
33	GIN			700		mV
34	SCL	High	2.0		5.0	V
		Low	GND		0.8	V
35	R_GND					
36	PC_5V					



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37	RIN			700		mV
38	VGA_CON					
39	GND					
40	GND					

6.5 Interface Timings

The signal interface of the TFT-LCD module is analog RGB compatible.

6.5.1 Timing Characteristics

The timings are supported by the signal interface of M240UP01 are listed as following table.

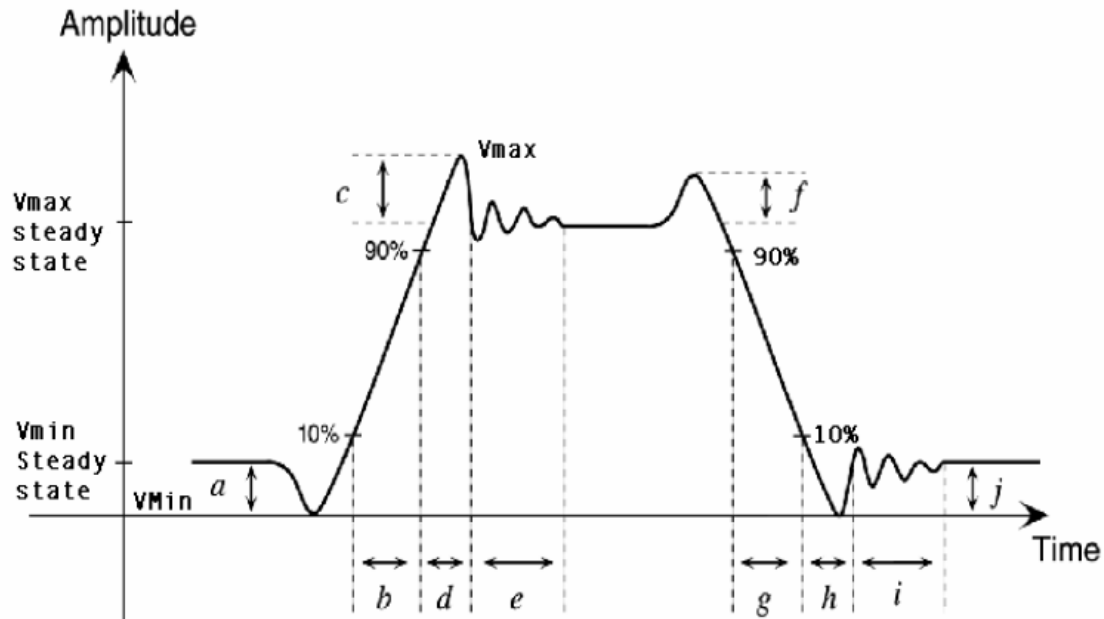
Resolution	Horizontal Frequency (KHz)	Vertical Frequency (Hz)	Dot Clock (MHz)	Actually Display Resolution	Remark
640x350	31.47(P)	70.08(N)	25.17	1920 x1200	DOS
720x400	31.47(N)	70.08(P)	28.32	1920 x1200	DOS
640x480	31.47(N)	60.00(N)	25.18	1920 x1200	DOS
640x480	35.00(N)	67.00(N)	30.24	1920 x1200	Macintosh
640x480	37.86(N)	72.80(N)	31.5	1920 x1200	VESA
640x480	37.50(N)	75.00(N)	31.5	1920 x1200	VESA
800x600	37.88(P)	60.32(P)	40	1920 x1200	VESA
800x600	48.08(P)	72.19(P)	50	1920 x1200	VESA
800x600	46.86(P)	75.00(P)	49.5	1920 x1200	VESA
832X624	49.72(N)	74.55(N)	57.29	1920 x1200	Macintosh
1024x768	48.36(N)	60.00(N)	65	1920 x1200	VESA
1024x768	56.48(N)	70.10(N)	75	1920 x1200	VESA
1024x768	60.02(P)	75.00(P)	78.75	1920 x1200	VESA
1024X768	60.24(N)	74.93(N)	80	1920 x1200	Macintosh
1152x864	67.50(P)	75.00(P)	108	1920 x1200	VESA
1152x870	68.68(N)	75.06(N)	100	1920 x1200	Macintosh
1152x900	61.80(N)	66.00(N)	94.5	1920 x1200	SUN 66
1152x900	71.81(N)	76.14(N)	108	1920 x1200	SUN
1280x1024	64.00(P)	60.00(P)	108	1920 x1200	VESA
1280x1024	75.83(N)	71.53(N)	128	1920 x1200	IBM1
1280x1024	80.00(P)	75.00(P)	135	1920 x1200	VESA
1280x1024	81.18(N)	76.16(N)	135.09	1920 x1200	SPARC2
1680x1050	64.7(P)	59.883(N)	119	1920 x1200	VESA
1680x1050	65.29(N)	59.954(P)	146.25	1920 x1200	VESA
1920x1200	74.04(P)	60(N)	154	1920 x1200	VESA
1920x1200	74.56(N)	60(P)	193.25	1920 x1200	VESA

Note-1: Depend on firmware setting. For D-sub, It can support other resolution when Dot Clock <210MHZ.
And DVI for Dot Clock <165MHZ

Note-2: “P”, “N” stands for “Positive”, “Negative” polarity of incoming H-sync/V-sync (input timing)

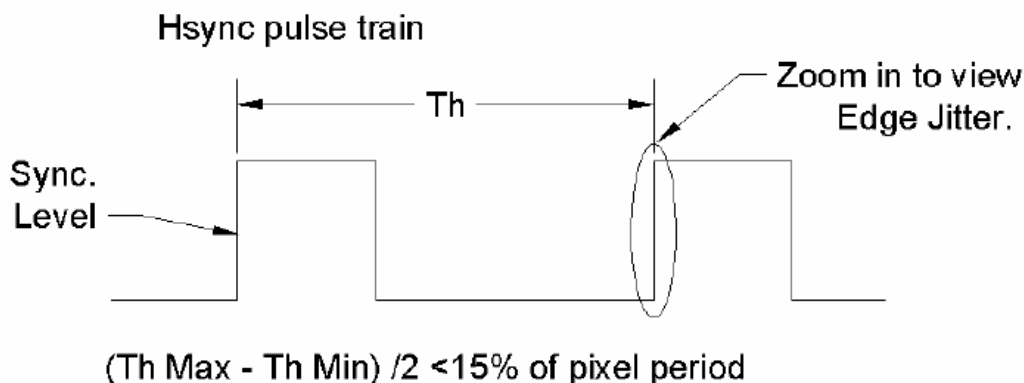
6.5.2 Definition of terms

➤ Video Signal Definition



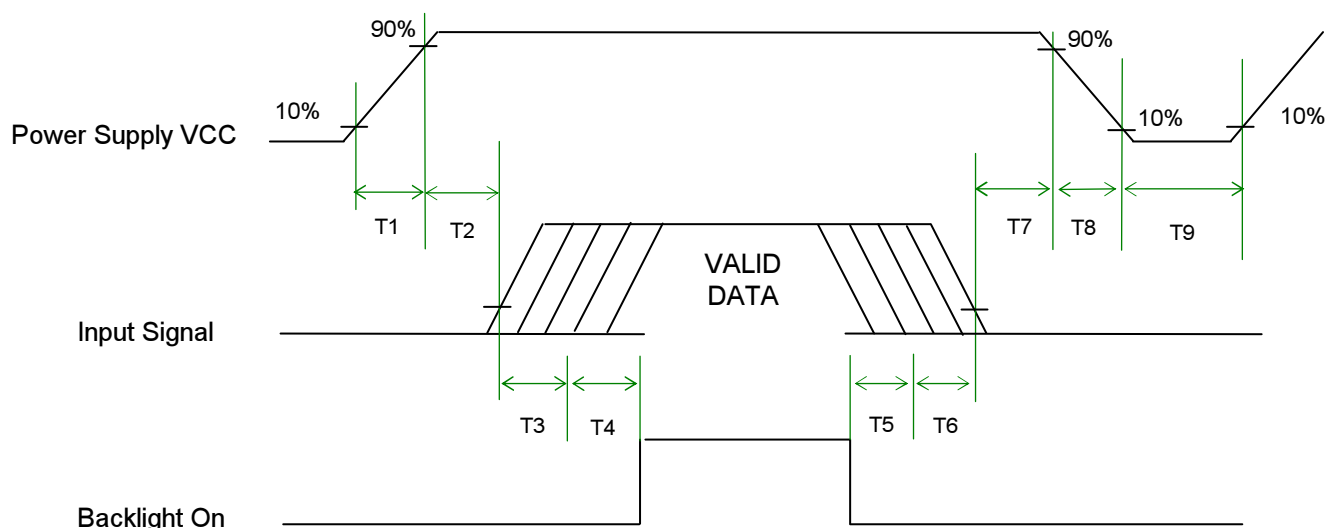
- a) Vmin steady state Amplitude before transition
- b) Video Rise Time Delta (t), (measured from the 10% to 90% points of Vmin Steady State to Vmax Steady State)
- c) Overshoot Amplitude
- d) Undefined
- e) Settling Time - Measured from the end of the overshoot to the point where the amplitude of the video ringing is down to $\pm 5\%$ of the final steady state value
- f) Undefined
- g) Video Fall Time Delta (t), (measured from the 90% to 10% points of Vmax Steady State to Vmin Steady State)
- h) Undefined here, Note: Undershoot is within this period and with an Amplitude of (j)
- i) Settling Time - Measured from the end of the undershoot to the point where the amplitude of the video ringing is down to $\pm 5\%$ of the final steady state value
- j) Vmin steady state Amplitude after transition

➤ Synchronization Signal Definition



6.6 Power ON/OFF Sequence

VCC power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VCC is off.



Power Sequence Timing

Parameter	Value			Unit
	Min.	Typ.	Max.	
T1	-	-	10	[ms]
T2	10	-	50	[ms]
T3 (Black pattern only)	30	-	50	[ms]
T4	200	-	-	[ms]
T5	200	-	-	[ms]
T6 (White pattern only)	50	-	100	[ms]
T7	0	16	50	[ms]
T8	-	-	100	[ms]
T9	1000	-	-	[ms]



7. Connector & Pin Assignment

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

7.1.1 Connector

Connector Name / Designation	Power / OSD Connector / J1
Manufacturer	STM or compatible
Type / Part Number	STM-MDS240315A
Mating Housing / Part Number	STM-PD240315

Connector Name / Designation	DVI-D / D-sub Connector / J2
Manufacturer	STM or compatible
Type / Part Number	STM-MDS240320A
Mating Housing / Part Number	STM-PD24320-2



7.1.2 Pin Assignment

➤ Power / OSD Connector (J1)

Pin#	Signal Name	Pin#	Signal Name
1	VCC	2	BKLT_ADJ
3	VCC	4	BKLT_EN
5	VCC	6	AUDIO_EN
7	VCC	8	MUTE
9	GND	10	VOLUME
11	GND	12	Key_Power
13	GND	14	MENU
15	GND	16	PLUS
17	S/PDIF	18	MINUS
19	I2CSDA	20	DOWN
21	I2CSCL	22	UP
23	SD0	24	SELECT
25	WS	26	SOURCE
27	SCK	28	LED_A
29	MCK	30	LED_G



➤ DVI-D / D-sub Connector (J2)

Pin#	Signal Name	Pin#	Signal Name
1	DATA2/4 Shield	2	GND
3	DATA2+	4	DVI_5V
5	DATA2-	6	HPD
7	GND	8	GND
9	DATA1+	10	DDC Data
11	DATA1-	12	DDC Clock
13	DATA1/3 Shield	14	GND
15	DATA0+	16	VCC
17	DATA0-	18	HDMI_HDP
19	DATA0/5 Shield	20	2D_SW
21	Clock+	22	DVI_CONN
23	Clock-	24	GND
25	Clock Shield	26	VSync
27	B_GND	28	HSync
29	BIN	30	GND
31	G_GND	32	SDA
33	GIN	34	SCL
35	R_GND	36	PC_5V
37	RIN	38	VGA_CON
39	GND	40	GND

8. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50□, 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50□, 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0□, 300hours	
High Temperature Storage (HTS)	Ta= 60□, 300hours	
Low Temperature Storage (LTS)	Ta= -20□, 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 G Wave: Random Frequency: 10 - 200 - 10 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Drop Test	Height: 38 cm, package test	
Thermal Shock Test (TST)	-20□/30min, 60□/30min, 100 cycles	1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	2
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:10,000 ft Non-Operation:30,000 ft	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

9. Shipping Label

The shipping label format is shown as below.

 *XXXXXXXXXXXX-XXXX*  XXXXXXXXXXXXXXXXXXXX	Manufactured XX/XX Model No: M240UP01 V.0 AU Optronics XXXXX MADE IN XXXXXX (XX)	 
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10. Mechanical Characteristics

	
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